EXHIBIT F

Correspondence

Tradeoff Between Threshold Voltage and Breakdown in High-Voltage Double-Diffused MOS Transistors

M. D. POCHA, J. D. PLUMMER, AND J. D. MEINDL

Abstract—**The design of junction isolated DMOS transistors suitable for monolithic integration has been studied. The purpose of this correspondence is to describe one of the key tradeoffs when designing these devices for high breakdown voltages (200 V for our example). It is a tradeoff primarily between threshold voltage and the punchthrough voltage of the channel diffusion, however, the avalanche breakdown voltage, on-resistance, and source-to-substrate punchthrough voltage are also affected. As an example, the design of a device for 200-V operation is described. The discussion is, however, general and can be applied to other DMOS designs as well.**

I. Introduction

High-voltage double-diffused MOS (DMOS) transistors have been fabricated in monolithic integrated circuits operating at voltages up to 200 V, for a new ultrasonic imaging system [1]. In the course of design and development of these transistors, several of their characteristics have been studied in detail. Three major areas of study have been 1) effects of device processing on threshold voltage, 2) current–voltage behavior, and 3) breakdown voltage. Work in the first two areas has already been reported [2], [3]. The purpose of this correspondence is to describe a particular set of tradeoffs which relate threshold voltage to the primary junction breakdown mechanisms in the high-voltage DMOS structure.

A cross-sectional view of the type of device being considered in this correspondence is shown in Fig. 1. This device is capable of switching 200-V peak-to-peak analog signals with peak currents on the order of 0.3 A [4]. The overall dimensions of the device are roughly 570 μm by 470 μm. The channel width is 2040 μm and channel length is approximately 3 μm. Some of the other important physical parameters are

1) p^- substrate resistivity	10–20 $\Omega \cdot$ cm
2) n^- epitaxial resistivity	5–7 $\Omega \cdot$ cm
3) epitaxial thickness	25–30 μm
4) p^+ contact junction depth	5 μm
5) channel junction depth	4.5 μm
6) n^+ source–drain junction depth	1.5 μm
7) gate oxide thickness	0.3 μm
8) field oxide thickness	1.5 μm.

The previous work on threshold voltage [2] showed that the threshold voltage is determined by the maximum net surface impurity concentration in the channel N_a (max). The study of current voltage behavior [3] showed that on-resistance of the device is dominated by the resistance of the drift region between the channel diffusion and the drain contact for high-voltage designs. This resistance was, furthermore, shown to be inversely proportional to the impurity concentration in the epitaxial layer N_d. In this correspondence we show that the drain-to-source punchthrough voltage is also affected by N_a (max) and can, therefore, be related to the threshold voltage. This punchthrough voltage also is a function of the epitaxial layer impurity concentration thereby providing a link to on-resistance, avalanche breakdown voltage, and source-to-substrate punchthrough voltage.

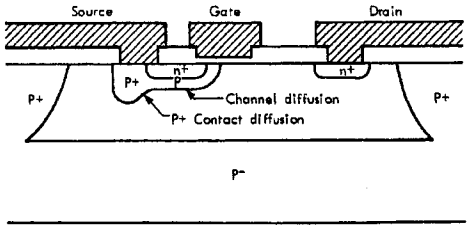

Fig. 1. Cross-sectional structure of a high-voltage DMOS transistor.

The optimization procedure in designing these devices is as follows. First, select the highest epitaxial layer concentration N_d, to minimize on-resistance, consistent with the desired avalanche breakdown voltage (200 V in our case). Using this value for N_d the net peak impurity concentration in the channel N_a (max) necessary to prevent source–drain punchthrough can be calculated for a given channel length. From N_a (max) a minimum threshold voltage can be calculated. Finally, from N_d a minimum epitaxial thickness to prevent source-to-substrate punchthrough can be calculated.

II. Punchthrough Breakdown Between Source and Drain

Punchthrough breakdown can occur whenever the depletion layer of one junction spreads until it reaches the depletion region of another junction [5]. One of the most important punchthrough mechanisms in high-voltage DMOS devices is that of the channel diffusion under the gate. Although the depletion layer of the channel–drain junction spreads primarily into the more lightly doped drain drift region, the shortness of the channel raises the possibility of punchthrough due to the small amount of spreading of the depletion layer into the more heavily doped channel region. An approximate calculation of this punchthrough voltage can be made by assuming a linear distribution of impurity in the channel diffusion and uniform distribution in the epitaxial layer. Assuming complete ionization, the electric field and voltage drop across the depletion layer can be calculated by solving Poisson's equation in one dimension.

The total punchthrough voltage is given by

$$V_R = \frac{q}{\epsilon_s}\left(\frac{N_a(\max)}{6} + \frac{N_a^2(\max)}{8N_d}\right)x_A^2. \quad (1)$$

Equation (1) shows the following: 1) The punchthrough voltage is proportional to the square of the channel length

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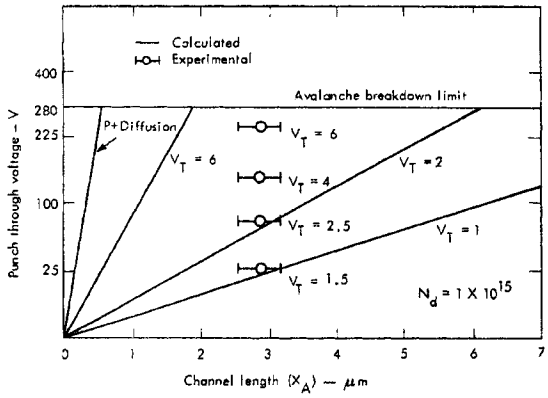

Fig. 2. Calculated and measured source-drain punchthrough voltage for an erfc profile and 5-Ω · cm epitaxial layer.

x_A^2. 2) The numerator of (1) contains N_d (max), which we recall determines the threshold voltage [2]. Devices with higher threshold voltage will, therefore, have higher punchthrough voltages. 3) The denominator of V_R contains N_d, the epitaxial concentration. Devices with lower epitaxial doping will, therefore, have higher punchthrough voltages.

The approximate impurity distribution used to develop the analytical expression in (1) gives an intuitive understanding of the relationship between the channel length, the maximum doping concentration, and the breakdown voltage. Based on theoretical work by Kennedy and O'Brien [6], the lateral impurity profile in the channel diffusion is thought to be more accurately described by the complementary error function (erfc) [2]. Fig. 2 shows the results of breakdown-voltage calculations obtained by numerically integrating the more accurate impurity profiles. In this figure, the source-to-drain punchthrough voltage is plotted on a square-root scale versus channel length with threshold voltage and epitaxial concentration as parameters. The threshold voltage was calculated for a 3000-Å gate oxide necessary for 200-V gate-to-source dielectric breakdown. The horizontal line at the top of the figure is the limiting avalanche breakdown voltage of the drain channel junction calculated using a simple critical field model. The diagonal lines are the punchthrough voltages. For example, in Fig. 2 a device having 3-μm channel length and 1-V threshold voltage will exhibit punchthrough at 25-V drain-to-source and a threshold voltage of over 4 V is necessary to increase the punchthrough voltage to greater than 200 V. Equation (1) shows that punchthrough voltage increases as the impurity concentration of the epitaxial layer decreases. Intuitively, this is because the depletion layer spreads more into the n region when it is more lightly doped. If (1) is used directly to make plots similar to Fig. 2, the calculated punchthrough voltages appear 20 to 50 percent higher than those in Fig. 2 for a given channel length and threshold voltage.

Experimental measurements of punchthrough voltage have been made on several devices with different threshold voltages. Their approximate channel lengths were then obtained from the impurity distributions. The results, plotted on Fig. 2, are in good agreement with the calculations except for the $V_T = 6$ V value discussed below. These experimental devices exhibit the classic "soft breakdown" characteristic associated with punchthrough at low values of threshold voltage and "hard breakdown" associated with avalanche at high threshold voltage [7]. Also, in Fig. 2 is plotted a line for the depletion layer of the more heavily doped p^+ source contact diffusion (Fig. 1) showing that the depletion layer spreads less than 1 μm into this diffusion before avalanche breakdown occurs.

The experimental measurements for the $V_T = 6$ V case are somewhat lower than the theoretical results, as the breakdown occurs due to avalanche in this case and is influenced by surface effects.

III. Punchthrough Breakdown Between Source and Substrate

The source-to-substrate punchthrough is of importance when the DMOS device is used as an analog multiplexer, or in any application in which the source is biased above the p^- substrate. The punchthrough is actually from the p^+ contact to substrate, but the source is generally connected to the p^+ contact to prevent back-gate bias effects. This punchthrough can occur when both source and drain are at a high positive potential with respect to the substrate. As the potential difference is increased, the depletion layer of the substrate-to-epitaxy junction spreads upward into the epitaxial region and downward into the substrate. The nearest junction is the p^+ contact diffusion so that, when the depletion layer reaches this junction's depletion region, punchthrough occurs.

Again the width of this depletion layer can be calculated by solving Poisson's equation for the required voltage. The result for our case $N_d = 1 \times 10^{15}$ cm^{-3} and 200 V is a depletion layer width in the epitaxial layer of 18.0 μm. Since the p^+ contact is approximately 5 μm deep, the total epitaxial layer thickness must be over 23 μm. To allow some tollerance for processing variations, the epitaxial layer is targetted at 25–30 μm.

IV. Discussion of Results

The results of the preceding discussions can be summarized as follows. Study of threshold voltage indicates that it is determined by the maximum net impurity concentration in the channel region N_A (max) and that processing variation effects can be minimized by a sufficiently long channel length and a minimum value of threshold voltage [2]. Study of source–drain punchthrough shows that it is also a function of N_d (max) resulting in a lower bound for threshold voltage for a given breakdown and epitaxial layer concentration N_d. However, by reducing N_d, the lower bound on the threshold voltage can also be reduced. N_d relates source–drain breakdown to another punchthrough breakdown from source to substrate when the DMOS device is used as an analog multiplexer. The source-to-substrate punchthrough determines the thickness of the epitaxial material required for a given breakdown voltage. This required epitaxial layer thickness increases as N_d decreases. The increase in epitaxial layer thickness requires deeper isolation diffusions, therefore, increasing the device size and processing time.

The increased size and processing time are, however, minor considerations, since the major effect of reducing N_d is on the electrical properties of the DMOS transistor. In the previously published discussion of the current–voltage behavior of these devices it was shown that the high-voltage DMOS structure could be modeled as an n-channel enhancement MOSFET in series with a fixed resistor [3]. The value of this series resistance is inversely proportional to N_d since it physically arises from the n^- drift region between the channel and the drain n^+ diffusion. Therefore, decreasing N_d results in an increase in the on-resistance of the DMOS device. The effect of N_d on source–drain punchthrough and minimum threshold voltage is not as pronounced, and therefore N_d should be made as large as possible. The upper limit of N_d is determined by avalanche breakdown of the p-type bulk channel diffusion to the n^- epitaxial layer. Fig. 2 shows that the theoretical avalanche breakdown for this junction with $N_d = 1 \times 10^{15}$ cm^{-3} is about 280 V implying that a higher value of N_d could be used. However, due to surface effects, the actual breakdown

voltage of these junctions range from 225 to 250 V. Thus the target value $N_d = 1 \times 10^{15}$ cm^{-3} is approximately the maximum epitaxial layer concentration for 200-V operation allowing for some variations in processing.

V. Conclusion

Tradeoffs between threshold voltage, punchthrough voltage, avalanche breakdown voltage, and on-resistance in the high-voltage DMOS structure have been discussed. It is shown that a maximum epitaxial layer concentration (to minimize on resistance) of 1×10^{15} cm^{-3} is consistent with a 200-V avalanche breakdown voltage requirement. This value of N_d leads to a minimum threshold voltage constraint of 4 V to obtain a drain-to-source punchthrough voltage of greater than 200 V. Finally, an epitaxial layer thickness greater than 23 μm is necessary for source-to-substrate punchthrough voltage greater than 200 V when the device is used as an analog multiplexer. While these results are based on a 200-V breakdown constraint, the calculations are sufficiently general to apply to other designs as well.

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Corner Currents in p$^+$-n-n$^+$ Diodes with n$^+$ Isolation Diffusions

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Abstract—**The magnitude of corner currents in rectangular diffused p$^+$-n-n$^+$ diodes with deep n$^+$ isolation diffusions is discussed. Curves are given to illustrate the importance of this current in diodes and IIL structures.**

I. Introduction

Recent papers [1], [2] give results which enable prediction of radial currents from circular diodes or corner currents from rectangular diodes made by one p$^+$ diffusion into an epitaxial layer on an n$^+$ substrate. It has been shown that in both cases, the additional current components can be an appreciable fraction of the normal "vertical" current due to injection and recombination within the n epitaxial layer between the p$^+$-n and the n-n$^+$ junctions. In this correspondence, we give results which enable prediction of the corner current when the rectangular diode is surrounded by an n$^+$ isolation diffusion extending down to the n$^+$ substrate. In particular, the effect of varying the distance of the n$^+$ isolation from the edge of the p$^+$ diffusion is considered. This technique is widely used in IIL structures for isolation purposes.

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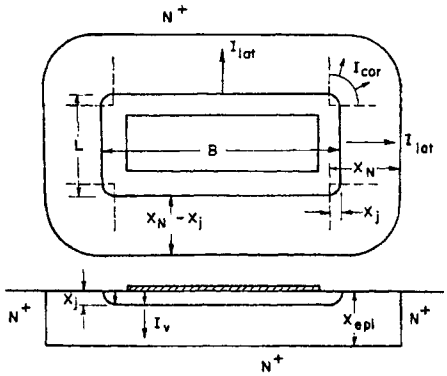

Fig. 1. p$^+$-n-n$^+$ diode with deep n$^+$ isolation diffusion.

II. Calculation of the Corner and Lateral Currents

Referring to Fig. 1, the p$^+$-n junction depth is X_j, the n-n$^+$ junction is at a distance X_{epi} from the surface, and the n-n$^+$ isolation is at a distance $X_N - X_j$ from the p$^+$-n junction. The simplifying assumption is made that the n-n$^+$ isolation is equidistant from the p$^+$-n junction at all points along the periphery and that the hole current is zero at the n-n$^+$ interface.

For an injected carrier concentration $p(0)$ at every point along the periphery and in the bulk, at the depletion layer boundary, the vertical current is given by

$$I_v = qBLp(0)(X_{epi} - X_j)/\tau \tag{1}$$

where τ is the minority carrier lifetime in the epitaxial layer and q the electronic charge. B and L are the dimensions of the p diffused region.

The current diffusing laterally from the junction is given by

$$I_{lat} = 2q(B + L)\, p(0)\, X_{epi}(D_p/L_p) \tanh [(X_N - X_j)/L_p] \tag{2}$$

where $L_p = D_p\tau$.

For the case where $X_N - X_j \ll L_p$, (2) simplifies to

$$I_{lat} = 2q(B + L)\, p(0)\, X_{epi}(X_N - X_j)/\tau. \tag{3}$$

In order to calculate the corner current, we must solve the continuity equation in cylindrical coordinates

$$\frac{d^2p}{dr^2} + \frac{1}{r}\frac{dp}{dr} - \frac{p}{L_p^2} = 0 \tag{4}$$

the boundary condition being $I_p = 0$ at $r = X_N$ (assuming an ideal "reflecting" n-n$^+$ interface), and hence $dp/dr = 0$ at $r = X_N$. The general solution to this equation involves a linear combination of the modified Bessel function of the first kind of order zero and the modified Bessel function of the third

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